REMARKS

Claims 1-17 remain pending in the application.

Claims 1-17 over Frampton, Perets and Feemster

In the Office Action, claims 1-17 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Pat. No. 5,802,351 to Frampton ("Frampton") in view of U.S. Pat. No. 5,537,576 to Perets et al. ("Perets") and further in view of Feemster et al. ("Feemster"). The Applicants respectfully traverse the rejection.

Claims 1-7 recite first and second mailbox portions **both** defined at least in part over **common** memory addresses, the first mailbox addressably filling upward through to a **highest** physical address of the common memory, and the second mailbox addressably filling downward through to a **lowest** physical address of the common memory. Claims 8-17 recite a **contiguous** block of **shared** memory, a first mailbox addressably filling upward through to a **highest** physical address of the **common** memory, and a second mailbox addressably filling downward through to a **lowest** physical address of the **common** memory.

With respect to the three cited references, Frampton teaches a data interface wherein a dual port memory forms nothing more than a conventional buffer by filling up from the bottom to the top. This arrangement is quite conventional. Even the Examiner admits that Frampton fails to teach filling downward toward a low physical address. (Office Action at 2)

The Examiner cites Perets to allegedly cure this first deficiency. In particular, the Examiner cites Perets, col. 6, lines 32-41; and col. 8, lines 40-52, as allegedly teaching "filling downward toward a low physical address." Perets teaches **expandable** memory for a digital signal processor. According to Perets, memory BANKS may be ADDED, e.g., in blocks of 64K, to fill in an otherwise EMPTY addressable section between upper and lower blocks.

The Examiner cites col. 4, lines 4-16 of Feemster as allegedly curing yet another deficiency in the combination of Frampton and Perets, i.e., a first processor as not having access to a second mailbox.

Nevertheless, even the combination of Frampton, Perets and Feemster if properly combined (which they are not with respect to claims 1-17) would still not teach a shared memory mailbox wherein a second mailbox portion addressably fills downward through to a **lowest physical address**, as claimed by claims 1-17.

Examiner's Response to Previous Arguments

The Examiner appears to correctly interpret Frampton, Perets, and Feemster. What it appears the Examiner may be misinterpreting are the requirements of claims 1-17.

In particular, on page 6, the Examiner interprets Perets such that it "maintains that the first memory bank 14 grows/fills from FFFF(hex) towards FE00(hex) (line 36) and that the second memory bank 15 grows/fills from 0 towards 0CFF(hex) (line 37)."

The Applicants agree.

What the Examiner may not have appreciated is that NEITHER OF THOSE MEMORY ADDRESS BLOCKS **OVERLAP**. These are TOTALLY SEPARATE BLOCKS OF MEMORY.

Claims 1-17 require first and second mailbox portions **both** defined at least in part over **COMMON** memory **ADDRESSES**. None of the addresses in the two memory block areas taught by Frampton, Perets or Feemster **OVERLAP**.

The Examiner appears to have interpreted claims 1-17 as requiring a "common boundary" as he has used that language twice at the bottom of page 6 of the Office Action. Claims 1-17 say nothing about a "common boundary". Claims 1-17 require defined memory block areas that **OVERLAP**.

Accordingly, for at least all the above reasons, claims 1-17 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

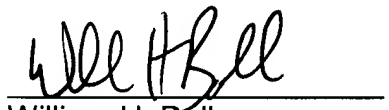
Telephone Interview Requested

The undersigned respectfully requests a telephonic interview with the Examiner at his convenience to clarify issues and perhaps overcome this apparent misunderstanding or misinterpretation of the claims 1-17.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



William H. Bollman
Reg. No. 36,457

Manelli Denison & Selter PLLC
2000 M Street, NW
Suite 700
Washington, DC 20036-3307
TEL. (202) 261-1020
FAX. (202) 887-0336